

Howard L. Bernstein

T (202) 663-7937 hbernstein@sughrue.com

August 27, 2003

z100 Pennsylvania Avenue, NW Washington, DC 20037-3213 T 202.293.7060 F 202.293.7860

> 1010 El Camino Real Menlo Park, CA 94025-4345

> > T 650.325.5800 F 650.325.6606

Toei Nishi Shimbashi Bldg. 4F 13-5 Nishi Shimbashi 1-Chome Minato-Ku, Tokyo 105-0003 Japan

> T 03.3503.3760 F 03.3503.3756

www.sughrue.com

MAIL STOP PATENT APPLICATION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Re:

Application of Shinya WATANABE and Hiroyuki KATOU

SEMICONDUCTOR CHIP HAVING AN ARRAYED WAVEGUIDE

GRATING AND METHOD OF MANUFACTURING THE

SEMICONDUCTOR CHIP AND MODULE CONTAINING THE

SEMICONDUCTOR CHIP

Assignee: NEC CORPORATION

Our Ref: Q76956



Dear Sir:

This is a request for a Divisional Application of pending prior Application No. 10/067,320 (Confirmation No.4597) filed February 7, 2002 of Shinya WATANABE and Hiroyuki KATOU entitled SEMICONDUCTOR CHIP HAVING AN ARRAYED WAVEGUIDE GRATING AND METHOD OF MANUFACTURING THE SEMICONDUCTOR CHIP AND MODULE CONTAINING THE SEMICONDUCTOR CHIP.

This application is being filed under 37 C.F.R. § 1.53(b). Enclosed is a specification, including the claims and abstract, 10 sheets of drawings, and a copy of the Declaration as filed in the prior application.

The prior application is assigned to Group Art Unit 2818.

Priority is claimed from:

Country

Application No

Filing Date

JAPAN

46663/2001

February 22, 2001

The priority document was filed in parent Application No. 10/067,320.

The Government filing fee is calculated as follows:

Total claims

9 - 20

=____ x

\$18.00 =

\$.00

Independent claims

2 - 3

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Base Fee

\$750.00

TOTAL FILING FEE

\$750.00



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A check for the statutory fee of \$750.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this transmittal letter is attached.

The application is timely filed.

Respectfully submitted,

SUGHRUE MION, PLLC Attorneys for Applicant

Howard L. Bernstein Registration No. 25,665

SUGHRUE MION, PLLC Telephone: (202) 293-7060 Facsimile: (202) 293-7860

WASHINGTON OFFICE 23373
CUSTOMER NUMBER